IN THE CLAIMS:

Claims 1, 3-4, 6-7 and 10-13 have been amended herein. All of the pending claims 1 through 13 are presented, pursuant to 37 C.F.R. §§ 1.121(c)(1)(i) and 1.121(c)(3), in clean form below. Please enter these claims as amended. Attached is a marked-up version of the claims amended herein pursuant to 37 C.F.R. § 1.121(c)(1)(ii).

1. (Amended) A semiconductor device comprising:
at least one layer of boro-phospho silicate glass; and
at least one layer of germanium boro-phospho silicate glass having at least a portion thereof contacting at least a portion of said at least one layer of boro-phospho silicate glass.

2. A semiconductor device comprising:
a plurality of layers of boro-phospho silicate glass; and
a plurality of layers of germanium boro-phospho silicate glass, at least a portion of at least one layer of said plurality of layers of germanium boro-phospho silicate glass contacting at least a portion of at least one layer of said plurality of layers of boro-phospho silicate glass.

3. (Amended) A semiconductor device comprising:
a plurality of layers of boro-phospho silicate glass; and
a plurality of layers of germanium boro-phospho silicate glass, each layer of said plurality of layers of germanium boro-phospho silicate glass having at least a portion thereof contacting at least a portion of at least one layer of said plurality of layers of boro-phospho silicate glass.

4. (Amended) A semiconductor memory device comprising:
at least one layer of boro-phospho silicate glass; and

at least one layer of germanium boro-phospho silicate glass having at least a portion thereof contacting at least a portion of said at least one layer of boro-phospho silicate glass.

5. A semiconductor memory device comprising:

a plurality of layers of boro-phospho silicate glass; and

a plurality of layers of germanium boro-phospho silicate glass, at least a portion of at least one layer of said plurality of layers of germanium boro-phospho silicate glass contacting at least a portion of at least one layer of said plurality of layers of boro-phospho silicate glass.

6. (Amended) A semiconductor memory device comprising:

a plurality of layers of boro-phospho silicate glass; and

a plurality of layers of germanium boro-phospho silicate glass, each layer of said plurality of layers of germanium boro-phospho silicate glass having at least a portion thereof contacting at least a portion of at least one layer of said plurality of layers of boro-phospho silicate glass.

7. (Amended) A semiconductor memory device comprising:

at least one capacitor cell having a portion thereof formed by at least one layer of boro-phospho silicate glass and at least one layer of germanium boro-phospho silicate glass having at least a portion thereof contacting at least a portion of said at least one layer of boro-phospho silicate glass.

8. A semiconductor memory device comprising:

at least one capacitor cell having a portion thereof formed by a plurality of layers of boro-phospho silicate glass and a plurality of layers of germanium boro-phospho silicate glass, at least a portion of at least one layer of said plurality of layers of germanium boro-

phospho silicate glass contacting at least a portion of at least one layer of said plurality of layers of boro-phospho silicate glass.

9. A semiconductor memory device comprising:

at least one capacitor cell having a portion thereof formed by a plurality of layers of boro-phospho silicate glass and a plurality of layers of germanium boro-phospho silicate glass, each layer of germanium boro-phospho silicate glass having at least a portion thereof contacting at least a portion of at least one layer of said plurality of layers of boro-phospho silicate glass.

10. (Amended) The memory device of claim 9, further comprising:

at least one dielectric layer; and

a conductive layer over said at least one dielectric layer.

11. (Amended) The memory device of claim 10, wherein said at least one dielectric layer comprises one of Si_3N_4, Ta_2O_5, or BST.

12. (Amended) The memory device of claim 10, wherein said conductive layer comprises Si-Ge.

13. (Amended) The memory device of claim 9, further comprising:

at least one dielectric layer covering at least portions of said plurality of layers of boro-phospho silicate glass and said plurality of layers of germanium boro-phospho silicate glass; and

a conductive layer covering at least a portion of said at least one dielectric layer.